EXHIBIT 13

External Memory Interface Handbook Volume 2: Design Guidelines

For UniPHY-based Device Families

Updated for Intel® Quartus® Prime Design Suite: **17.0**

2. DDR2 and DDR3 SDRAM Board Design Guidelines

The following topics provide guidelines for improving the signal integrity of your system and for successfully implementing a DDR2 or DDR3 SDRAM interface on your system.

The following areas are discussed:

- comparison of various types of termination schemes, and their effects on the signal quality on the receiver
- proper drive strength setting on the FPGA to optimize the signal integrity at the receiver
- effects of different loading types, such as components versus DIMM configuration, on signal quality

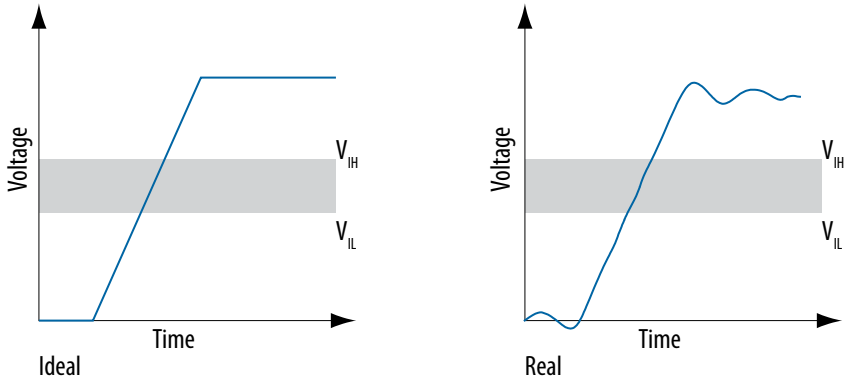
It is important to understand the trade-offs between different types of termination schemes, the effects of output drive strengths, and different loading types, so that you can swiftly navigate through the multiple combinations and choose the best possible settings for your designs.

The following key factors affect signal quality at the receiver:

- Leveling and dynamic ODT
- Proper use of termination
- Layout guidelines

As memory interface performance increases, board designers must pay closer attention to the quality of the signal seen at the receiver because poorly transmitted signals can dramatically reduce the overall data-valid margin at the receiver. The following figure shows the differences between an ideal and real signal seen by the receiver.

Figure 10. Ideal and Real Signal at the Receiver



2.1. Leveling and Dynamic Termination

DDR3 SDRAM DIMMs, as specified by JEDEC, always use a fly-by topology for the address, command, and clock signals.

Intel recommends that for full DDR3 SDRAM compatibility when using discrete DDR3 SDRAM components, you should mimic the JEDEC DDR3 fly-by topology on your custom printed circuit boards (PCB).

Note: Arria® II, Arria V GX, Arria V GT, Arria V SoC, Cyclone® V, and Cyclone V SoC devices do not support DDR3 SDRAM with read or write leveling, so these devices do not support standard DDR3 SDRAM DIMMs or DDR3 SDRAM components using the standard DDR3 SDRAM fly-by address, command, and clock layout topology.

Table 24. Device Family Topology Support

Device	I/O Support
Arria II	Non-leveling
Arria V GX, Arria V GT, Arria V SoC	Non-leveling
Arria V GZ	Leveling
Cyclone V GX, Cyclone V GT, Cyclone V SoC	Non-leveling
Stratix III	Leveling
Stratix IV	Leveling
Stratix V	Leveling

Related Information

www.JEDEC.org

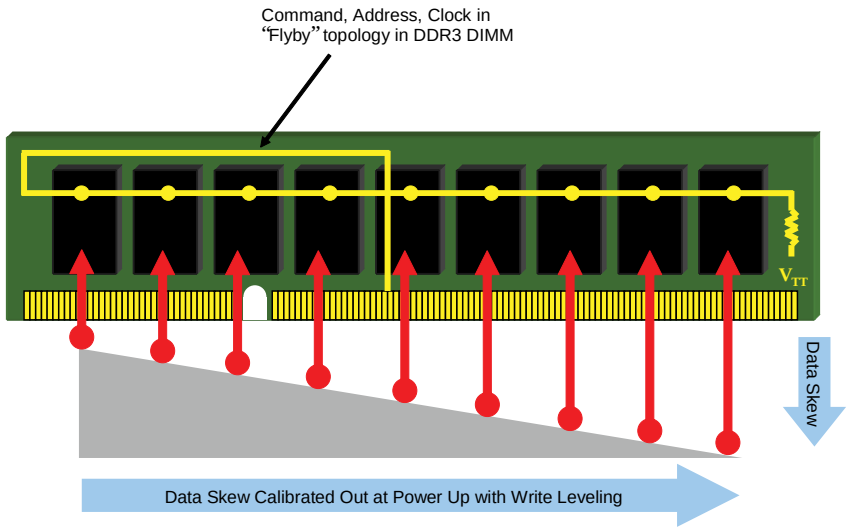
2.1.1. Read and Write Leveling

A major difference between DDR2 and DDR3 SDRAM is the use of leveling. To improve signal integrity and support higher frequency operations, the JEDEC committee defined a fly-by termination scheme used with clocks, and command and address bus signals.

The following section describes leveling in DDR3.

Fly-by topology reduces simultaneous switching noise (SSN) by deliberately causing flight-time skew between the data and strobes at every DRAM as the clock, address, and command signals traverse the DIMM, as shown in the following figure.

Figure 11. DDR3 DIMM Fly-By Topology Requiring Write Leveling



The flight-time skew caused by the fly-by topology led the JEDEC committee to introduce the write leveling feature on the DDR3 SDRAMs. Controllers must compensate for this skew by adjusting the timing per byte lane.

During a write, DQS groups launch at separate times to coincide with a clock arriving at components on the DIMM, and must meet the timing parameter between the memory clock and DQS defined as tDQSS of ± 0.25 tCK.

During the read operation, the memory controller must compensate for the delays introduced by the fly-by topology. The Stratix® III, Stratix IV, and Stratix V FPGAs have alignment and synchronization registers built in the I/O element to properly capture the data.

In DDR2 SDRAM, there are only two drive strength settings, full or reduced, which correspond to the output impedance of 18-ohm and 40-ohm, respectively. These output drive strength settings are static settings and are not calibrated; consequently, the output impedance varies as the voltage and temperature drifts.

The DDR3 SDRAM uses a programmable impedance output buffer. There are two drive strength settings, 34-ohm□and 40-ohm . The 40-ohm drive strength setting is currently a reserved specification defined by JEDEC, but available on the DDR3 SDRAM, as offered by some memory vendors. Refer to the data sheet of the respective memory vendors for more information about the output impedance setting. You select the drive strength settings by programming the memory mode register defined by mode register 1 (MR1). To calibrate output driver impedance, an external precision resistor, RZQ, connects the ZQ pin and VSSQ. The value of this resistor must be 240-ohm ± 1%.

If you are using a DDR3 SDRAM DIMM, RZQ is soldered on the DIMM so you do not need to layout your board to account for it. Output impedance is set during initialization. To calibrate output driver impedance after power-up, the DDR3 SDRAM needs a calibration command that is part of the initialization and reset procedure and is updated periodically when the controller issues a calibration command.

In addition to calibrated output impedance, the DDR3 SDRAM also supports calibrated parallel ODT through the same external precision resistor, RZQ, which is possible by using a merged output driver structure in the DDR3 SDRAM, which also helps to improve pin capacitance in the DQ and DQS pins. The ODT values supported in DDR3 SDRAM are 20-ohm , 30-ohm , 40-ohm , 60-ohm , and 120-ohm , assuming that RZQ is 240-ohm.

Related Information

www.JEDEC.org

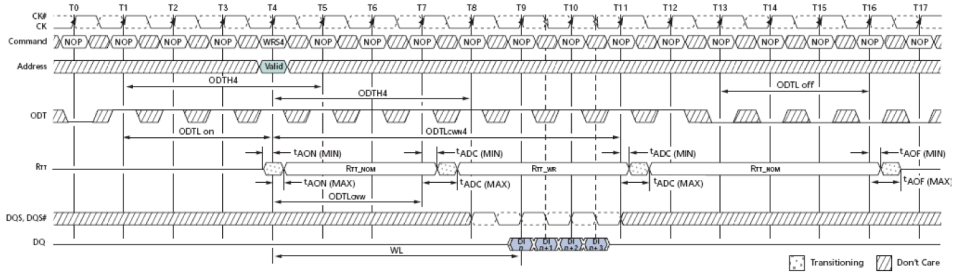
2.1.2. Dynamic ODT

Dynamic ODT is a DDR3 SDRAM feature that is not available in DDR2 SDRAM. Dynamic ODT can change the ODT setting without issuing a mode register set (MRS) command.

When you enable dynamic ODT, and there is no write operation, the DDR3 SDRAM terminates to a termination setting of RTT_NOM; when there is a write operation, the DDR3 SDRAM terminates to a setting of RTT_WR. You can preset the values of RTT_NOM and RTT_WR by programming the mode registers, MR1 and MR2.

The following figure shows the behavior of ODT when you enable dynamic ODT.

Figure 12. Dynamic ODT: Behavior with ODT Asserted Before and After the Write



In the multi-load DDR3 SDRAM configuration, dynamic ODT helps reduce the jitter at the module being accessed, and minimizes reflections from any secondary modules.

For more information about using the dynamic ODT on DDR3 SDRAM, refer to the application note by Micron, *TN-41-04 DDR3 Dynamic On-Die Termination*.

Related Information

www.JEDEC.org

2.1.3. Dynamic On-Chip Termination

Dynamic OCT is available in Arria V, Cyclone V, Stratix III, Stratix IV, and Stratix V.

The dynamic OCT scheme enables series termination (RS) and parallel termination (RT) to be dynamically turned on and off during the data transfer. The series and parallel terminations are turned on or off depending on the read and write cycle of the interface. During the write cycle, the RS is turned on and the RT is turned off to match the line impedance. During the read cycle, the RS is turned off and the RT is turned on as the FPGA implements the far-end termination of the bus.